COURSE DESCRIPTION CARD - SYLLABUS

Course name
Programmable Digital Circuits [S1MiKC2>ProgUC]

Course

Field of study
Microelectronics and Digital Communication

Year/Semester
2/4

Area of study (specialization)
–

Profile of study
general academic

Level of study
first-cycle

Course offered in
Polish

Form of study
full-time

Requirements
compulsory

Number of hours

Lecture
24

Laboratory classes
30

Other
0

Tutorials
0

Projects/seminars
0

Number of credit points

4,00

Coordinators

dr hab. inż. Olgierd Stankiewicz prof. PP
olgierd.stankiewicz@put.poznan.pl

dr inż. Adam Grzelka
adam.grzelka@put.poznan.pl

Lecturers

Prerequisites

Has a basic knowledge of Boolean algebra. Has a knowledge in area of programming in C / C++. Has a general knowledge about combinational and sequential digital circuits. Has a general knowledge in area of binary arithmetic and digital representation of signals. Is able to look for information required during design process and take educational courses, if needed, especially through Internet and distance education. Knows the limitations of their own knowledge and skills; can precisely formulate questions; understands the need for further education and systematic reading of scietnific journals in the field. Can work individually and in team; knows the responsibility for tasked realized in team.

Course objective

The main purpose of the course is to show various design techniques for digital ciruits that can be suitable for ASIC/FPGA devices. As hardware description language the Verilog will be used. A lot of examples will show how to efficiently use all basic and generic FPGA blocks (like RAM, DSP, etc.). Laboratory work will be performed with exploiting FPGA boards.

Course-related learning outcomes

Knowledge:
Has basic knowledge of development trends in programmable circuits. K1_W11
Has sufficient knowledge to design specialized digital circuits for use in programmable circuits. K1_W02, K1_W03
Knows the principle of operation of basic communication interfaces. K1_W02
Knows the principles of design of basic elements of digital circuits (automata, pipelines). K1_W03

Skills:
It is able to obtain data from literature and other sources, can integrate obtained information, interpret it, as well as formulate and justify opinions. K1_U01
Can describe digital circuit elements in the form of Verilog language module. K1_U10
Can test and verify the correct operation of a digital circuit. K1_U11
Can use the learned design techniques to design a digital circuit .K1_U10
Has the ability to use modern tools to support the design and synthesis of digital circuits for the FPGA chip platform. K1_U11

Social competences:
It is open to opportunities for continuous learning and understands the need to improve professional competence. K1_K01
Has basic knowledge necessary to understand non-technical conditions of engineering activities; knows basic principles of occupational safety and health. K1_K02
Has a sense of responsibility for designed electronic and telecommunication systems. K1_K04

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

Lecture: written exams. The written exam consists of 6-10 closed and open questions. Each question is scored according to its complexity. A short descriptive answer is expected, or marking the correct answers of a closed question. Passing threshold: 50% of the points. Credit issues, based on which the questions are developed, will be sent to students by e-mail using the university e-mail system.
Laboratory: reports (Report) of thematically uniform blocks of laboratory exercises. Laboratory project carried out individually or in small groups.
The following percentage thresholds for individual grades apply to pass the lecture, laboratory and project: 2.0 (< 50%), 3.0 (50%-59%), 3.5 (60%-69%), 4.0 (70%-79%), 4.5 (80%-89%), 5.0 (90% and more).

Programme content

Lecture:
Introduction to digital programmable devices. General structrue of FPGA devices. Basic embedded blocks (RAM, PLL, FIFO, etc.). Comparison of different FPGA devices. Inter-domain communication (source-synchronous interface). High-speed I/O interfaces - Use Gigabit GTP, GTX, GTH modules in HD-SDI, SATA, PCI-E, and SerDes. Systems in Layout (SoC). Programming languages - Verilog, SystemC, SystemVerilog, migen, MyHDL. Principles of good programming, self-describing code.
Methods and tools for simulation and synthesis of projects on FPGA devices - EDIF file generation, project partitioning, Python scripting language.
Examples of effective implementation of selected algorithms (DCT conversion, RGB-YUV colour space conversion, elementing, composite multiplication, floating point operations), for FPGA devices.
Laboratories:
Simulation and synthesis framework and software. Basic testbenches. Design of various modules: random number generators. binary coded decimals converter, buffer modules (e.g. stack, fifo), arithmetic logic units, state machines. Design of a system comprising state machines, e.g. demonstration of traffic lights, or equ

Course topics

Consistent with the program content, including, among others: development of programmable circuits, historical outline, GAL, PAL, CPLD circuits, description of FPGA technology, circuit features, size, manufacturing technology, description of the main circuit families, structure of FPGA - basic cell (register, LUT), special elements: BRAM memories, DSP blocks, PLL clock manager, DCM, ADCM,

communication ports GTP, GTX, GTH, SerDes, techniques for designing digital circuits for FPGA circuits: effective use of DSP blocks and BRAM memories, Verilog language - basics, examples of design support systems, advanced versions of the language, design of basic structures of digital circuits - automata, pipelines, memory elements, FIFO, LIFO queues, examples in Verilog language, communication buses. Programming and testing of FPGA.

Teaching methods

Lecture: multimedia presentation with examples presented on the blackboard.
Laboratories: work on computers with simulation and synthesis software. Usage of FPGA boards. Examples illustrated on screen/blackboard.

Bibliography

Basic:
Skahill K., VHDL for Programmable Logic / Język VHDL , WNT, SBN-13: 978-0201895735, ISBN-10: 0201895730.
Giovanni De Micheli, Synthesis and Optimization of Digital Circuits / Synteza i optymalizacja układów cyfrowych , WNT, ISBN-13: 978-0070163331 ISBN-10: 00

Additional:
Łuba T., Rawski M., Tomaszewicz P., Zbierzchowski B., Synteza układów cyfrowych, Wydawnictwa Komunikacji i Łączności, Warszawa 2003.
Hajduk Z., Wprowadzenie do języka Verilog, BTC, Warszawa 2009.
Kamionka-Mikuła H., Małysiak H., Pochopień B., Synteza i analiza układów cyfrowych, WKŁ.Zbysiński P., Pasierbiński J.: Układy programowalne pierwsze kroki, Wydawnictwo BTC, Warszawa 2004,
Łuba T. Synteza układów logicznych. Oficyna Wyd. PW, Warszawa, 2005

Breakdown of average student's workload

	Hours	ECTS
Total workload	104	4,00
Classes requiring direct contact with the teacher	54	2,00
Student's own work (literature studies, preparation for laboratory classes/ tutorials, preparation for tests/exam, project preparation)	50	2,00